

Development of Low-THD Rippleless PFC Converter for High-Performance Electric Vehicle Charging

Adapa Sudheer Kumar^{1*}, V. Suresh², Daggi Veera Venkata Chaitanya³, Depati Veera Venkata Sai⁴, Gavara Sai Babu⁵

¹Assistant Professor, Department of Electrical and Electronics Engineering, Godavari Institute of Engineering and Technology(A), Rajahmundry.

²Assistant Professor, Department of Electrical and Electronics Engineering, Godavari Global University, Rajahmundry.

^{3,4,5}UG Scholar, Department of Electrical and Electronics Engineering, Godavari Institute of Engineering and Technology (A), Rajahmundry.

E-mail: 1*adapasudheer@giet.ac.in

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ABSTRACT

With the era of diversified automotive technologies, petrol and diesel motor vehicles have ruled supreme as the main modes of transportation for years. However, their adverse environmental impacts have propelled the world toward electrified mobility at a faster pace. Such a shift highlights the importance of a comprehensive study of critical building blocks of Electric Vehicles (EVs), more specifically vehicle charging stations. This paper presents a novel low-ripple Alternating Current (AC) – Direct Current (DC) conversion architecture for Electric Vehicle (EV) charging applications, integrating a Rippleless Power Factor Correction (PFC) stage with high-frequency galvanic isolation and synchronous rectification.

The front-end PFC circuit employs a dual-loop control mechanism combining a hysteresis current control strategy with voltage and current PI controllers. This approach ensures accurate input current shaping, reduced Total Harmonic Distortion (THD), and near-unity power factor, while providing stable and ripple-free DC output ideal for battery charging systems. The intermediate high-frequency inverter and isolation transformer enable compact design and safe voltage level adaptation, meeting safety and performance standards required in EV infrastructures. On the secondary side, a synchronous rectifier with closed-loop control minimizes switching losses and enhances energy transfer efficiency. The coordinated control structure ensures excellent dynamic response and robust output voltage regulation under

*Corresponding author.



varying input and load. Conditions, which are common in real-world EV charging scenarios MATLAB simulation results validate that the proposed system attains superior power quality, enhanced efficiency of 97.5%, and effective ripple suppression reduced THD of 1.17% compared to conventional converter topologies

تطوير محول تصحيح معامل القدرة (PFC) منخفض التشوه التوافقي الكلي (THD) وخالٍ من التموج لشحن المركبات الكهربائية عالية الأداء

ملخص: مع ظهور تقنيات السيارات المتنوعة، هيمنت سيارات البنزين والديزل على وسائل النقل الرئيسية لسنوات. إلا أن آثارها البيئية السلبية دفعت العالم نحو التنقل الكهربائي بوتيرة أسرع. يُبرز هذا التحول أهمية دراسة شاملة للمكونات الأساسية للسيارات الكهربائية، وتحديدًا محطات شحنها. تقدم هذه الورقة البحثية بنية جديدة لتحويل التيار المتردد إلى تيار مستمر منخفضة التموج لتطبيقات شحن السيارات الكهربائية، حيث تدمج مرحلة تصحيح معامل القدرة (PFC) الخالية من التموج مع عزل جلفاني عالي التردد وتقويم متزامن. تستخدم دائرة تصحيح معامل القدرة الأمامية آلية تحكم ثنائية الحلقة تجمع بين استراتيجية تحكم تيار التخلف ووحدات تحكم تناسبية تكاملية (PI) للجهد والتيار. يضمن هذا النهج تشكيلًا دقيقًا لتيار الإدخال، وتقليل التشوه التوافقي الكلي (THD)، ومعامل قدرة قريب من الواحد، مع توفير خرج تيار مستمر مستقر وخالٍ من التموج، مثالي لأنظمة شحن البطاريات. يُتيح العاكس الوسيط عالي التردد ومحول العزل تصميمًا صغيراً وتكيفاً آمناً لمستوى الجهد، ما يلبي معايير السلامة والأداء المطلوبة في البنية التحتية للمركبات الكهربائية. في الجانب الثانوي، يُقلل مقوم متزامن ذو تحكم ذي حلقة مغلقة من فاقد التبديل ويُحسن كفاءة نقل الطاقة. يضمن هيكل التحكم المنسق استجابة ديناميكية ممتازة وتنظيمًا قويًا لجهد الخرج في ظل ظروف الإدخال والحمل المتغيرة، وهي ظروف شائعة في سيناريوهات شحن المركبات الكهربائية في العالم الحقيقي. تؤكد نتائج محاكاة MATLAB أن النظام المقترح يُحقق جودة طاقة فائقة، وكفاءة مُحسنة بنسبة 97.5%، وكبحاً فعالاً للتموج مع انخفاض نسبة التشوه التوافقي الكلي إلى 1.17% مقارنة بتصميمات المحولات التقليدية.

الكلمات المفتاحية: المركبات الكهربائية، مرحلة تصحيح معامل القدرة الخالية من التموج، التحكم في التيار بالتباطؤ، العاكس عالي التردد، محول العزل، المقوم المتزامن.

1. INTRODUCTION

A country's social and economic progress is directly correlated with the performance and efficiency of its transport infrastructure, as it is a critical channel of the exchange of goods, services, and ideas. Transportation systems, for all their utility, however, necessarily generate environmental and social issues, such as the emission of greenhouse gases and air pollution [1]. To counteract this, EVs have come into focus as a clean option, with lower carbon emissions and lower dependence on fossil fuels. Yet, one of the key technical issues related to EVs is their battery charging systems [2]. The majority of EVs employ uncontrolled rectifier-based power electronic converters to deliver DC power to the load, commonly controlled by voltage-mode or current-mode control policies. These uncontrolled charging strategies do not comply with global Power Quality (PQ) standards, especially with regard to the disturbances they inject at the AC mains interface [3]. The primary function of an EV charger is to regulate the switching of power electronic devices in an intelligent manner, based on reliable measurement of the battery's internal resistance and coordinated control of circuit components. Unfortunately, traditional chargers tend to produce substantial THD, causing a distorted harmonic profile at the grid interface. To meet PQ standards, EV chargers need to keep input current THD under 5% and provide a smooth harmonic spectrum [4].

Normally, an EV battery charger involves a Diode Bridge Rectifier (DBR) converting AC input to unregulated DC followed by an isolated DC-DC converter to convert it into

regulated output [5]. But with different load conditions, these systems have low power factor and poor input current quality, which negatively impacts battery health and charging efficiency. In high-power applications, conduction losses in the DBR further decrease system efficiency. The passive filters minimize THD, yet their effect on power factor is negligible, and their size is cumbersome for high-power systems [6, 7]. Better suited as an alternative, PFC converters have been developed as the predominant charging interface. These converters not only overcome size and efficiency limitations but also provide a stable and regulated DC output with good power quality indices at grid side [8].

Generally, an AC–DC rectifier circuit is utilized to convert utility AC voltage to a useful DC output. Such simple rectifier circuits, though, have limited conduction intervals, leading to a low input power factor [9, 10]. To counteract harmonic distortion and enhance power quality, PFC stage is generally implemented in front of the primary power conversion system. The typical two-stage PFC topology is comprised of a separate PFC stage and an isolated DC–DC converter. Of all topologies, boost converter is most commonly used for PFC applications because it directly regulates the line current and generate a continuous, low-distortion input current waveform [11].

1.1. Related works

Kai Yao *et al* (2021) [12] have implemented a boost PFC converter for utilizing in low power applications. Due to their many benefits, such as zero-current switch turn-on, no reverse recovery in diode and simple control, boost PFC converters are primarily used. At high input voltages, the input current of a standard boost PFC converter is distorted by the third harmonic which has a 180° phase shift from the fundamental one. Hengguo Zhang *et al* (2023) [13] have offered single phase AC/DC boost converter for realizing PFC. Because it shapes input current and achieve high PF for medium-to-high power single-phase AC–DC applications. On the other hand, it necessitates strict output voltage control. Henrique Marin van der Broocke Campos *et al* (2022) [14] have presented a switched-capacitor PFC boost rectifier for enhancing power quality in the load. Low voltage gain switched-capacitor PFC boost rectifier that provides intrinsic capacitor voltage balancing without the use of an external control loop. But it utilizes more parts in the power stage, which makes it heavier and more expensive. K. Thirupura Sundari *et al* (2023) [15] have introduced non-ideal quadratic boost PFC converter for providing uninterruptible DC power. Because it can provide the high voltage gain needed during wind speed fluctuations while guaranteeing less switching stress, increased efficiency, positive output polarity, and efficient electrical isolation, a quadratic boost converter is used. However, input voltage is polarized in the other direction and current is irregular. Haci Bodur *et al* (2022) [16] have developed a single-stage single switch isolated AC-DC PFC topology for attaining high efficiency. This approach thus realizes a high duty cycle, reduces current stress and improves efficiency, but in their isolated structure, it inevitably face the problems of increased design complexity, higher component count, and additional transformer-related losses. Pingjuan Niu *et al* (2025) [17] have designed totem-pole bridgeless PFC, uses Triangular Current Mode (TCM) control along with coordinated interleaved parallel operation that enables full-range zero-voltage switching (ZVS), lower inductor current ripple and less device stress. Yet, the dependency on TCM

control lead to higher current ripple and make the design more complicated for higher-power scalability. Arun Kumar Pallekonda *et al* (2024) [18] have presented a high gain interleaved PFC converter. The converter achieves an improved efficiency and excellent ripple minimization, yet scaling-up and costs might be a couple of difficulties of hardware realization due to the interleaved structure.

The contributions of the proposed high performance EV charging system are:

- AC source input is facilitated from the grid with sinusoidal voltage profile as the basis for PFC and harmonic elimination.
- Rippleless PFC converter offers regulated low-THD DC output with unity power factor, ensuring efficient power transfer and minimal ripple for battery charging.
- The hysteresis controller with voltage and current controller enables accurate input current shaping and dynamic voltage regulation by dual-loop control, improving power quality and system stability.
- Single-phase high-frequency inverter traverses DC to high-frequency AC allowing compact transformer design and the ability to galvanically isolate for safe EV charging.
- Isolation transformer provides electrical isolation between the grid and vehicle-side circuitry while converting voltage levels to accommodate varied battery specifications.
- Synchronous rectifier eliminates switching loss and enhances conversion efficiency through the use of actively controlled switches instead of passive diodes to provide ripple-free DC output.

The rest of this paper is organized as follows: Section II present block diagram of new EV charging system, with emphasis on the functional tasks of the Rippleless PFC converter, high-frequency inverter, isolation transformer, synchronous rectifier, and control loops. Section III outlines the system modelling, while Section IV shows simulation results and performance analysis that prove the effectiveness of the system for minimizing THD and enhancing power factor under different load conditions. Section V concludes the paper through abstracting the main findings, discussing design constraints, and providing recommendations for future improvements to scalable and intelligent EV charging infrastructure.

2. BLOCK DIAGRAM DESCRIPTION

This research addresses the growing demand for high-performance of EV charging systems integrating power factor correction, galvanic isolation and dynamic voltage regulation. The proposed block diagram comprises of rippleless PFC converter, single-phase high-frequency inverter, isolation transformer, synchronous rectifier, and integrated control approach as displayed in Figure.1.

The AC power attained from the grid is the primary energy source, which consists of harmonics due to non-linear load and grid fluctuations. The converter is utilized for mitigating these distortions for suppressing high-frequency noise. The rippleless PFC based converter is proposed that performs AC-DC conversion, while ensuring low THD and unity power factor. The dual loop control approach composed of hysteresis current controller with voltage and current PI controller. Converter switching frequency is regulated by the hysteresis current controller, ensuring input current within a specified hysteresis band. Voltage PI controller controls DC bus voltage by comparing output voltage measurement against a reference and producing an error signal. This error is processed to correct the duty

cycle of switching pulses. Current PI controller also ensures that amplitude of input current is exactly as desired, helping maintain accurate power factor correction. The PWM generator generates switching pulses from the hysteresis and PI controllers' control signals. These pulses are used to drive the active switches on the PFC converter to make efficient modulation and suppression of ripple.

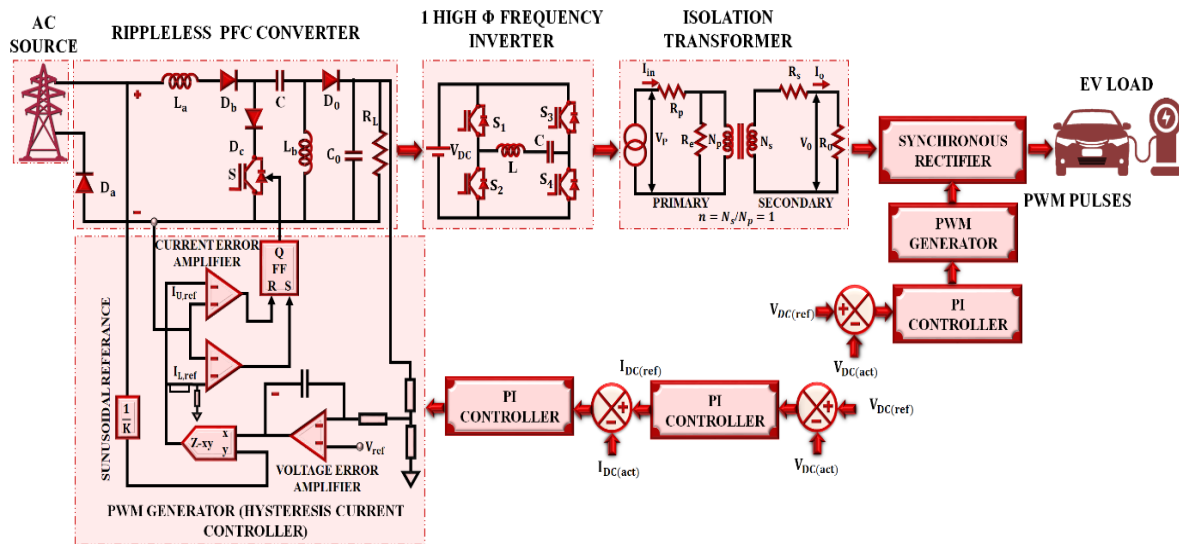


Figure 1. Proposed high performance EV charging system.

The result of this stage is a ripple-free, regulated DC voltage that is used as input to high-frequency inverter. The PFC stage's regulated DC output is supplied to a single-phase high-frequency inverter. Inverter produces high-frequency AC from DC voltage, allowing galvanic isolation. The inverter is operated in closed-loop control for maintaining waveform integrity and switching efficiency. It employs sinusoidal PWM modulation to produce high-frequency AC signals with minimal distortion. The inverter's high-frequency AC output is connected to a galvanic isolation transformer. This transformer offers electrical isolation between vehicle-side and grid-side circuitry, providing user safety and EV charging standards compliance. High-frequency AC output of transformer is converted back into DC using a synchronous rectifier. This phase **substitute's** traditional diode-based rectification with active switching devices regulated through PWM. The last output of the converter is supplied to the EV battery via the load interface. This phase has filtering components to suppress any remaining ripple and guard against voltage spikes on the battery. The system is meant to operate under varying load conditions, such as changes in battery state-of-charge, ambient temperature, and grid fluctuations.

3. PROPOSED SYSTEM MODELLING

3.1. Rippleless PFC Converter

This research proposes a novel AC/DC rippleless PFC converter topology that efficiently reduces the THD and improves the Power Factor (PF) at a low implementation cost. The proposed rippleless converter combines the bridge rectification and DC/DC conversion stages into a single stage using only one active switch (S). Consequently, the system cost is minimized. In contrast to the traditional converter that has a greater number of active switches, the new configuration adopts additional diodes (D_a, D_b, D_c, D_0) in the current path

to avoid short-circuit situations and minimize the overall number of expensive active switches. Being passive and less expensive compared to switches, this translates to even lower costs.

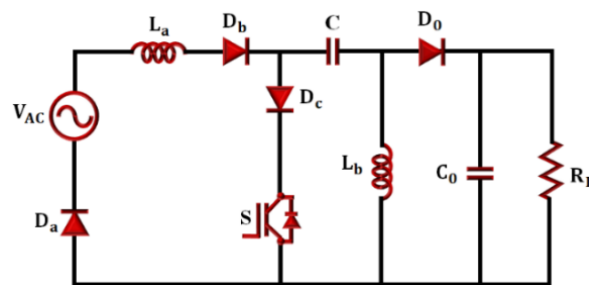


Figure 2. Rippleless PFC converter.

As illustrated in Figure. 2, the proposed PFC makes use of a single switch S that operates during entire cycle of the input voltage. Two blocking diodes D_a and D_c ensure appropriate isolation and prevent conduction conflict due to positive as well as negative half cycles of AC input voltage.

While input voltage is in positive half cycle, input current flows through inductors (L_a, L_b) when S is turned ON. Current in L_a rises proportionally, controlled by the impressed AC source voltage. Meanwhile, capacitor C is charged and inductor L_b interacts with the output capacitor C_0 to provide a ripple-free and smooth output voltage to the load R_L . The blocking diode D_b controls the flow of current and D_0 provides proper rectification to the DC output stage.

When S is OFF, stored energy in (L_a, L_b) gets discharged via the diodes and capacitors, thus transferring energy to the load R_L with negligible current ripple. This collaborative operation of inductors and capacitors provides ripple-free operation with high PF and low THD.

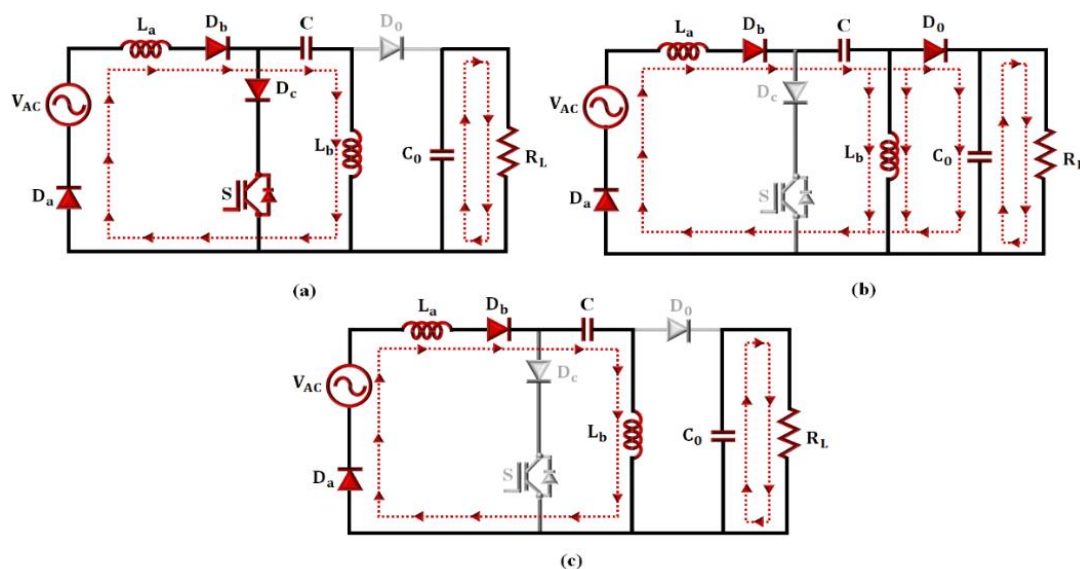


Figure 3. Modes of operation of proposed rippleless PFC converter (a) Mode 1 (b) Mode 2 (c) Mode 3.

Figure.3 depicts the modes of operation of proposed rippleless PFC converter within positive half-cycle of input AC voltage (V_{AC}), there are three different modes of operation of converter based on the switching state of S and the conducting status of the diodes (D_a, D_b, D_c, D_0).

Mode 1: When S is ON, D_c is in conduction while D_0 is reverse-biased. The input inductor current through L_a rises linearly with slope equal to $(-V_{AC}/L_a)$. In the meantime, the

capacitor C gets charged and energy is stored in L_b and C_0 to provide a regulated supply to load R_L .

$$i_{La}(t) = i_{La}(t_0) + V_{AC}(t_0)/L_a(t - t_0) \quad (1)$$

Mode 2: When S is OFF, D_b is forward biased and begins conducting, whereas diode D_0 offers a discharge path to the load. The current in inductor L_a reduces linearly with a slope of $(-V_0/L_a)$, where output voltage is V_0 . Concurrently, current in L_b rises linearly with a slope of $-V_0/L_b$. The related equation is:

$$i_{Lb}(t) = i_{Lb}(t_1) + V_0/L_a(t - t_1) \quad (2)$$

At this point, the condition between inductor currents is provided as:

$$i_{La} = i_{Lb} \quad (3)$$

Mode 3: When switch S is OFF and D_b is cut off, the stored energy in inductors L_a and L_b keeps supplying the load via C_0 and diode D_0 . During this freewheeling period, both inductors dump their stored energy until the next switching period. Thus, the current balance is given as:

$$i_{La}(t) = i_{Lb}(t) \quad (4)$$

For the proposed rippleless PFC converter, input peak current is determined as:

$$I_{in,peak} = \frac{P_0}{\eta \cdot V_{AC} \cdot \sqrt{2}} \quad (5)$$

$$\Delta I_{in} = 0.2 \times I_{in,peak} \quad (6)$$

The ripple current of inductor is represented as:

$$\Delta I = \frac{V_{AC} \cdot d}{L \cdot f_s} \quad (7)$$

Duty cycle is limited by:

$$\frac{V_0}{V_{AC} + V_0} \leq d \leq \frac{V_0}{V_{AC}} \quad (8)$$

The average current per switching cycle from the output is:

$$I_{DC,avg} = \frac{d^2 V_{AC}}{2LV_0 f_s} \quad (9)$$

Peak inductor current is:

$$I_{DC,peak} = i_{La}(t) + i_{Lb}(t) = \frac{V_{AC} \cdot d T_s}{L_a} + \frac{V_{AC} \cdot d T_s}{L_b} \quad (10)$$

Average output current per half-line cycle is:

$$I_{avg} = \frac{1}{T} \int_0^T i(t) dt \quad (11)$$

For $d = 0.2$, the equivalent inductance L_e is found to be:

$$L_e = \frac{(V_{AC} \cdot d)^2}{4V_0 f_s I_{avg}} \quad (12)$$

The input inductor value L_a is:

$$L_a = \frac{V_{AC} \cdot d}{f_s \cdot \Delta I} \quad (13)$$

The second inductor L_b is given as:

$$L_b = L_e - L_a \quad (14)$$

Lastly, the output capacitance needed to obtain a DC bus ripple that is specified is:

$$C_0 = \frac{P_{load}}{V_0^2 \cdot 4f_{ac} \cdot \Delta V_{bus}} \quad (15)$$

With volt-second balance on L_a and L_b (Rippleless PFC) in CCM:

Switch S , ON interval, $v_{La} = +v_g$, $v_{Lb} = -V_0$

Switch S , OFF interval, the diode D_0 conducts, $v_{La} = -V_C$, $v_{Lb} = V_C - V_0$

With $\langle v_{La} \rangle = \langle v_{Lb} \rangle = 0$ for one T_s and the coupling-capacitor average $V_C = \frac{D}{1-D}$.

For PFC operation with sinusoidal $v_{AC}(t) = V_m \sin \omega t$, the duty is modulated as

$$D(t) = \frac{V_0}{V_0 + |v_{AC}(t)|} \quad (16)$$

Such that input current is proportional to $|v_{AC}(t)|$.

In order to quantitatively demonstrate the ripple suppression capacity of the introduced rippleless PFC converter, a quantifiable Figure of merit in terms of peak-to-peak DC bus voltage ripple ratio is designated. Ripple ratio is given by,

$$\text{Ripple Ratio} = \frac{\Delta V_{bus(pp)}}{V_0} \quad (17)$$

Where, $\Delta V_{bus(pp)}$ is peak-to-peak ripple voltage across DC-link capacitor and V_0 is average DC output voltage. Due to synchronized energy exchange between inductors (L_a, L_b) and the highly efficient optimization of the output capacitor sizing C_0 , proposed converter is capable of keeping a very low ripple ratio even when subjected to load changes.

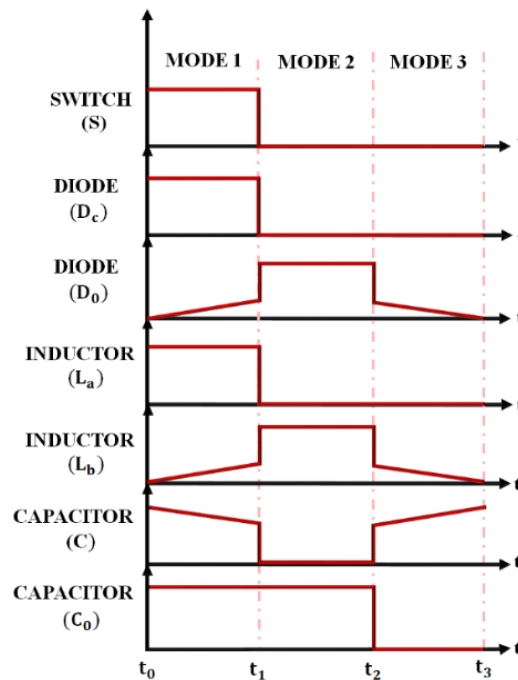


Figure 4. Timing Diagram.

Figure 4 illustrates the timing diagram of the proposed rippleless PFC converter, which efficiently boosts the AC input from the grid to a regulated DC output, thereby enhancing power delivery to the EV load.

3.2. PWM Generator (Hysteresis Controller)

In rippleless PFC converters, accurate current control is crucial to provide high power quality and efficient energy conversion, Figure.5. Among the various pulse-width

modulation PWM strategies, hysteresis band current control is frequently favoured due to its simplicity and ease of implementation. This method offers rapid dynamic response in the current loop and does not require prior knowledge of load parameters, making it highly adaptable across varying operating conditions.

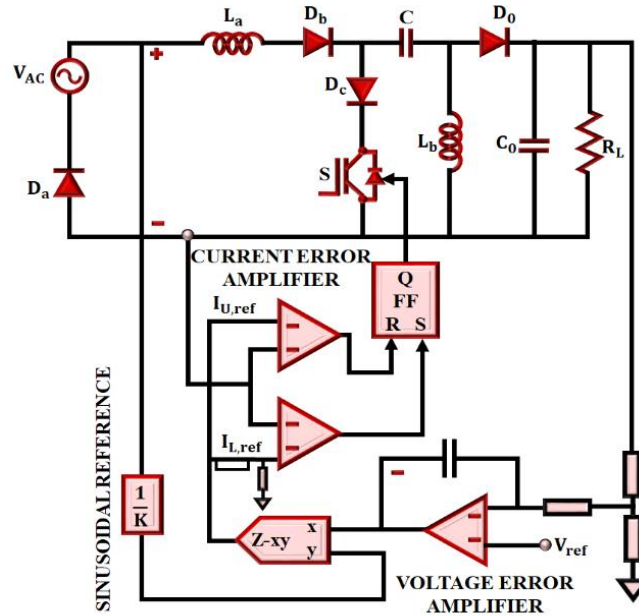


Figure 5. Closed loop rippleless converter using hysteresis control for PFC.

3.2.1. Control Architecture Overview

The control for a rippleless PFC converter generally involves two nested loops:

- Outer Voltage Control Loop
- Inner Current Control Loop

In outer loop, output voltage is constantly measured, scaled, and compared to a predetermined reference. The resultant error signal is treated by PI controller, which generates control signal that controls current reference.

3.2.2. Reference Current Synthesis

The reference current is synthesized by multiplying the sinusoidal voltage template extracted from the input supply with the PI controller output. This reference guides the inner current loop.

3.2.3. Hysteresis Current Control Mechanism

In hysteresis current control, two sinusoidal reference currents are defined based on upper and lower boundary thresholds. The switching logic operates as follows:

- When the inductor current drops below the lower reference limit ($I_{L(ref)}$), the switch is activated (ON).
- When current exceeds upper reference limit ($I_{U(ref)}$), switch is deactivated (OFF).

This system keeps current within hysteresis band, thus controlling the output of the converter and ensuring power quality.

Although hysteresis control provides a very good dynamic response and simplicity, it inherently produces a variable switching frequency. This is due to the requirement of keeping a consistent peak-to-peak current ripple during the fundamental frequency cycle. In order to

keep ripple in inductor current minimized, narrow hysteresis band is commonly chosen, as shown in Figure. 6.

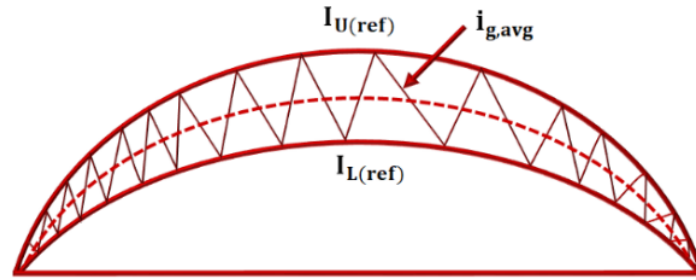


Figure 6. Hysteresis band.

3.2.4. Adaptive Hysteresis Band Adjustment Algorithm:

To solve the problem of fluctuating switching frequency that accompanies typical hysteresis control, a self-adaptive hysteresis band method is utilized in the present rippleless PFC converter. The instantaneous current error is figured out as,

$$e_i(t) = i_{ref}(t) - i_L(t) \quad (17)$$

Where, $i_{ref}(t)$ is the reference current generated by the outer voltage PI controller and $i_L(t)$ is measured inductor current.

Hysteresis band width $h(t)$ is adjusted dynamically depending on the magnitude of the current error and the operating conditions, and it is represented as

$$h(t) = h_{min} + k_h |e_i(t)| \quad (18)$$

where, h_{min} is minimum hysteresis band and k_h is adaptive gain. If load suddenly change due to any event, an increase in $e_i(t)$ widens the hysteresis band, thus, the current is tracked faster. When conditions are stabilized, the band becomes narrower, hence current ripple and switching losses decrease.

The switching frequency f_s is inversely proportional to the hysteresis band width, therefore,

$$f_s \propto \frac{1}{h(t)} \quad (19)$$

Upper and lower bounds are set on $h(t)$ to limit the switching frequency to a feasible range. Load changes are taken care of by the outer voltage loop since a change in load modifies $i_{ref}(t)$, which then affects the adaptive hysteresis band through the current error. This adaptive hysteresis, band PWM method ensures that the device is continuously working in a stable state, the ripple is lowered, and the efficiency is upgraded while a high-power factor is kept even with the grid and load varying.

Hysteresis current control offers a strong and flexible approach to controlling rippleless PFC converters. Its capability of keeping current within a closely regulated band without precise load information makes it well-suited to dynamic, uncertain environments. While variable switching frequency represents a challenge, adaptive hysteresis methods hold the promise of achieving optimized converter performance.

3.3. PI Controller

PI controller is a key component in determining output of proposed rippleless PFC converter for EV battery charging operation. The proposed controller compares carrier signal

with reference signal and produce a control output, further enhancing efficiency of entire system.

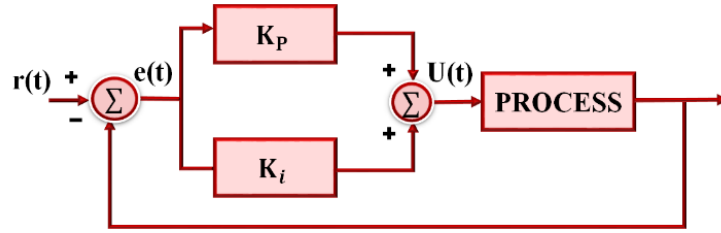


Figure 7. PI controller.

Figure 7 shows block representation of PI controller that is used in proposed EV charging architecture.

The PI controller generates the control signal $u(t)$, which contains two parts, the proportional response corresponding to instantaneous error signal $e(t)$ and integral response corresponding to the accumulated error over time, from the processed error signal that results from difference between reference value and measured output. This combination of these two actions provides very low steady- state error and stable regulation of converter output voltage, input current shaping and battery charging features. Mathematically, the error signal and controller output are represented by (17) and (18).

$$u(t) \propto [e(t) + \int e(t)dt] \quad (20)$$

$$u(t) = K_p e(t) + K_i \int e(t)dt \quad (21)$$

Here, the integral gain is indicated as $K_i \cos \theta_{A1}$ and the proportional gain is given by $K_i = -\omega_1 \sin \theta_{A1}$. These gains parameters are determined to provide fast dynamical response, low ripple and accurate reference signal tracking under load and input variations. Therefore, the PI controller transfer function is presented as in (19).

$$G_c(s) = \frac{U(s)}{E(s)} = K_p + \frac{K_i}{s} \quad (22)$$

3.3.1. Stability Analysis:

A small, signal modelling approach has been adopted to analyse the stability of the proposed dual-loop controlled rippleless PFC converter around the nominal operating point. The inner current control loop is given a higher bandwidth than the outer voltage loop to guarantee a good separation of the time scales and to avoid loop interaction. Frequency, domain analysis of the system reveals that the loops have sufficient gain and phase margins to perform stably under grid voltage variations and dynamic load conditions. Time-domain simulations also demonstrate system capability in operating stably and responding rapidly, with minimal overshoot, and robust regulation without oscillations, during sudden load and input disturbances. Hence, PI controller plays a vital role in operation of proposed rippleless PFC converter, thus leading to improved power quality and overall system efficiency.

3.4. Single Phase High Frequency Inverter

For the purposes of harmonic suppression and reactive power compensation, DC voltage from PFC converter is transformed to high-frequency AC through a specialized inverter. This process improves system efficiency and power quality. The working mechanism is as follows:

When the transmission system is at the resonant point, the input impedance of the switching power supply is purely resistive, resulting in input current being in phase with voltage waveform. PF is then unity, allowing for maximum output power transfer. This, however, results in a high level of harmonic content.

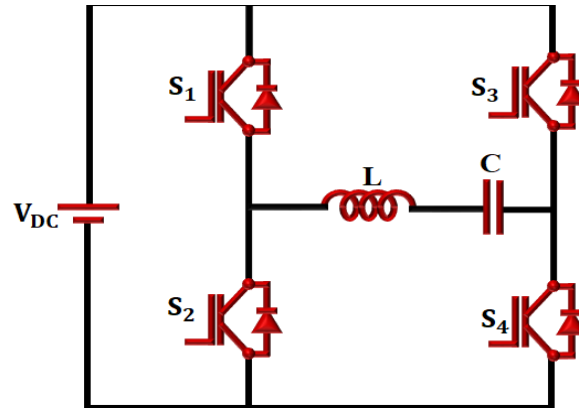


Figure 8. Single-phase high frequency inverter.

The inverter structure, as shown in Figure. 8, consists of four switches S_1 to S_4 . These switches switch in diagonal pairs: S_1 and S_2 switch together, and S_3 and S_4 switch together. This pattern of switching alternates the polarity of load voltage. Conduction time of these switches is modulated to convert DC input into a high-frequency AC output.

Configuration of inductors:

- Inductor L acts as the inverter's primary winding and aids energy transfer and shaping of resonance.
- Capacitor C serves both as a component of the EMI filter network and as a series compensator for the inverter primary coil.

Collectively, these components allow accurate voltage harmonics and reactive power control, helping ensure stable and efficient inverter operation.

3.5. Isolation Transformer

Power quality is fundamentally influenced by the rated operating conditions at the nodes of the power system that supply electrical loads. Optimal performance of electrical equipment is achieved when it operates under nominal voltage and within the permissible limits of other power quality parameters. Deviations from these ideal conditions lead to suboptimal functioning, manifesting as reduced efficiency, elevated power losses, or even operational disruptions. Significant voltage fluctuations from the rated value may trigger protective mechanisms or, in the absence of such safeguards, result in equipment failure.

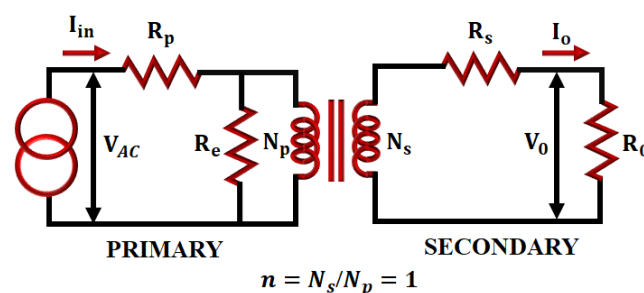


Figure 9. Isolation transformer circuit diagram.

The voltage transformation in the ideal isolation transformer, Figure.9 is controlled by the **turn's** ratio(n), given by:

$$n = \frac{N_p}{N_s} \tag{23}$$

Where, N_p is primary winding number of turns, N_s is number of turns in secondary winding. For a 1:1 isolation transformer, ($n = 1$) which means, $V_p = V_s$ and $I_s = I_p$ where, (V_p, I_p) are main voltage and current, (V_s, I_s) are secondary voltage and current. Transformer also adds an impedance that assists in dampening high-frequency transients. The equivalent circuit adds leakage inductance L_1 and winding resistance R_w , which assist in the voltage drop and filtering traits:

$$V_s = V_p(R_w \cdot I_p) + \omega(L_1 \cdot I_p) \tag{24}$$

Impedance performs as a low-pass filter, suppressing high-frequency disturbances and safeguarding downstream apparatus. Furthermore, isolation transformers play a crucial role in breaking ground loops, which are a prevalent source of Electromagnetic Interference (EMI). By removing direct electrical continuity between input and output grounds, they minimize the risk of circulating currents and related noise.

4. RESULT AND DISCUSSION

The proposed high performance EV system is implemented in MATLAB Simulink and simulation results with proposed rippleless PFC converter comparative analysis is presented below.

Table 1. Displays the parameter specifications.

Parameter	Specifications
AC Source	
AC Source Voltage	350V
AC Source Current	50A
Load Resistance	100Ω
Load Inductance	10mH
Rippleless PFC Converter	
Switching Frequency	10kHz
Capacitor (C)	22μF
Capacitor (C_0)	2200μF
Inductor (L_a, L_b, L_c)	4.7mH

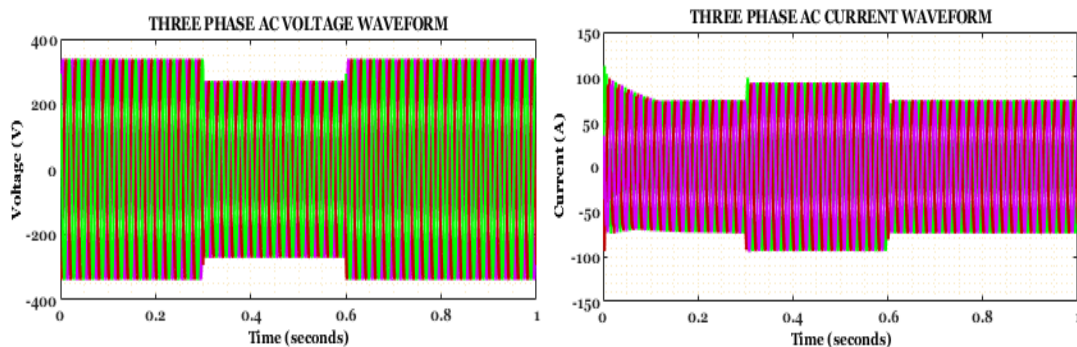


Figure 10. Three-phase AC source waveforms.

Figure.10 presents the dynamic behaviour of input voltage and current waveforms of three-phase AC source, utilized for operation of proposed low-THD rippleless PFC

conversion. The voltage waveform shows a sinusoidal shape, attaining voltage around $\pm 350V$ and around $0.3s$, there is a change in amplitude, indicating load variations. The current waveforms peaking at $\pm 50A$ both waveforms are shifted by 120° , showing the balanced three-phase power supply is symmetrical

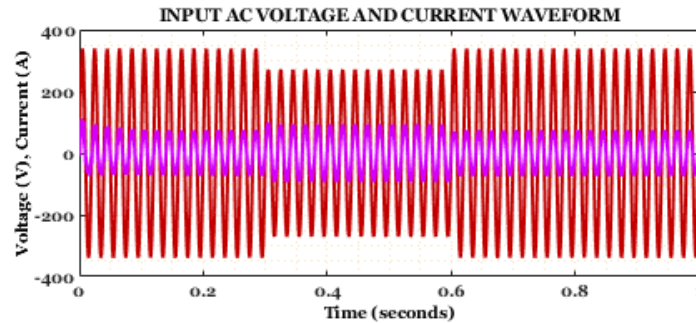


Figure 11. Input AC source waveform.

Figure. 11 represents input AC voltage and current waveforms in attaining proposed rippleless PFC approach. The voltage waveform exhibits a stable sinusoidal shape with voltage values reaching around $\pm 350V$, while the current waveform maintains a peak amplitude of $\pm 50A$. This near-perfect alignment between voltage and current confirms the **converter's ability to achieve unity power factor operation, thereby minimizing reactive power draw and enhancing grid compliance.** The absence of distortion and harmonic spikes in the current waveform further validates the low-THD performance of the system, which is critical for high-efficiency EV charging applications.

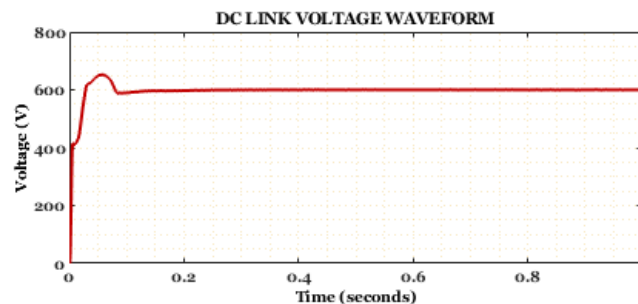


Figure 12. DC link voltage waveform.

Figure. 12 displays voltage waveform of the DC link, system attains a very stable DC link voltage profile, as indicated by the waveform. The voltage quickly stabilizes to around $600V$, showing fast transient response and less overshoot. During operation, the output is essentially ripple-free, crucial for the safety of EV batteries as well as enabling efficient energy transfer.

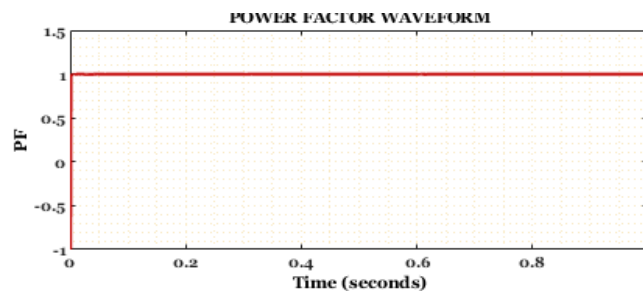


Figure 13. Power factor waveform.

Figure. 13 visualizes PF waveform of proposed ripples PFC converter incorporated into EV charging system. The power factor is always at unity (PF = 1) throughout the system. This flat-line response at PF = 1 ensures that input current is perfectly in phase with input voltage, showing zero reactive power and maximum real power transfer. This performance is a direct result of the converter's sophisticated control strategy, involving hysteresis current regulation and accurate PWM modulation.

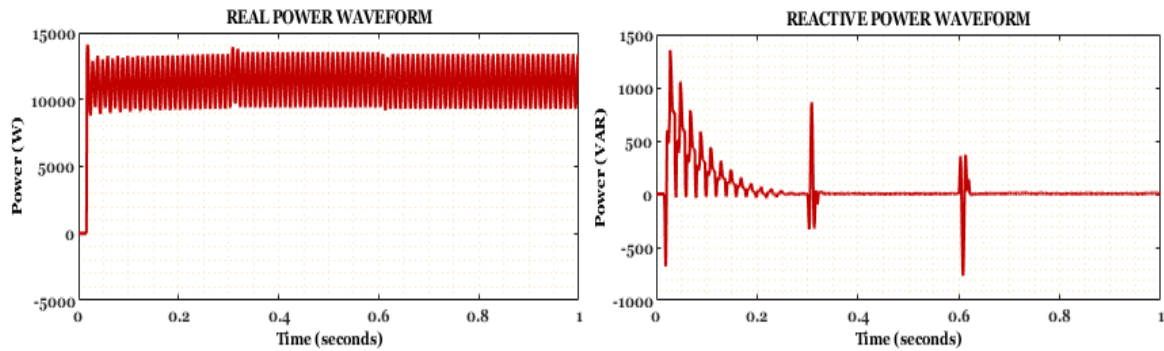


Figure 14. Real and reactive power waveform.

Figure. 14 illustrates response of real and reactive power profiles. Waveform of real power proves to deliver a consistent value with small high-frequency ripples common with fast switching actions in high-frequency inverters. This proves effective energy conversion and stable power supply to the load or utility grid. Conversely, the reactive power first shows transient oscillations, but rapidly stabilizes to close to zero. This observation again verifies that the control strategy successfully synchronizing the current with the voltage, thus maintaining close to unity power factor.

Figure. 15 demonstrates the voltage waveforms involved with a single-phase high-frequency inverter and isolation transformer, demonstrating the system's operating dynamics and performance tendencies. The inverter output voltage, around ± 500 V with high frequency is maintained throughout the system. Such a high-frequency switching scheme is characteristic of leading-edge inverter topologies optimized for high-efficiency DC-to-AC conversion.

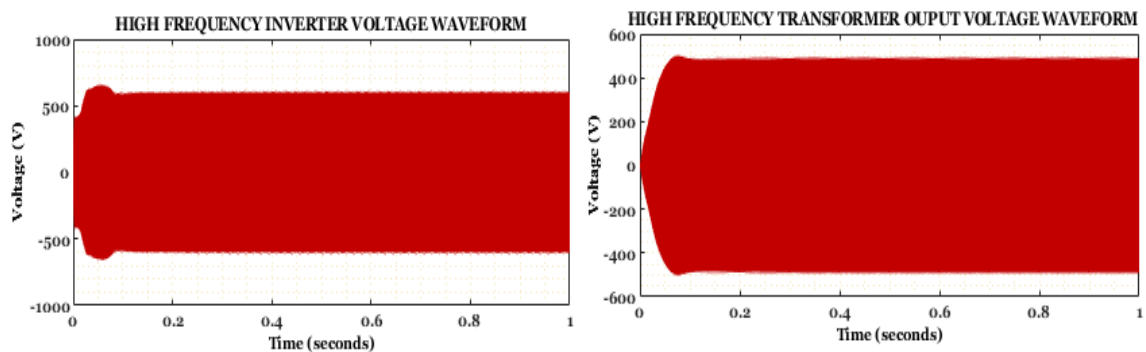


Figure 15. High frequency inverter and transformer waveforms.

The output voltage of the isolation transformer, which reduces the high-frequency signal of the inverter to a lower-amplitude range of about ± 400 V, validating the transformation's application to voltage scaling and galvanic isolation.

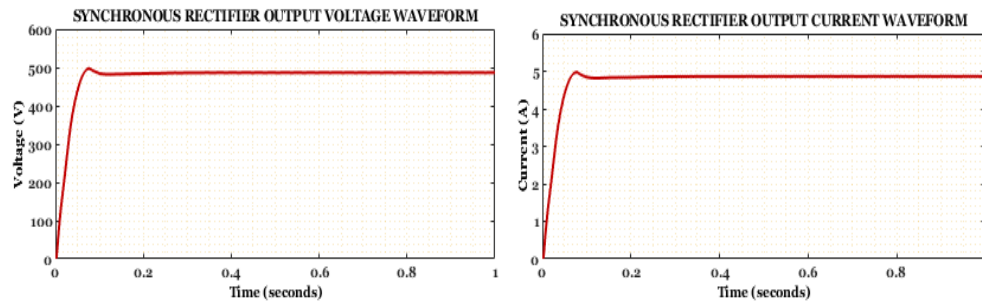


Figure 16. Synchronous rectifier waveforms.

Figure. 16 shows output voltage and current waveforms of synchronous rectifier stage of the innovative low-THD rippleless PFC converter for high-performance EV charging. The voltage waveform illustrates a steep rise to about 500V, then an extended, ripple-free profile over the duration observed, reflecting good DC conversion and voltage regulation. The output current waveform shows a rapid ramp-up to approximately 5 A and a smooth level with little ripple, affirming the converter's capability to provide smooth and stable charging current. The synchronous rectifier stage is a critical component in exhibiting high-quality power delivery, enhancing the overall ruggedness and reliability of the EV charging system.

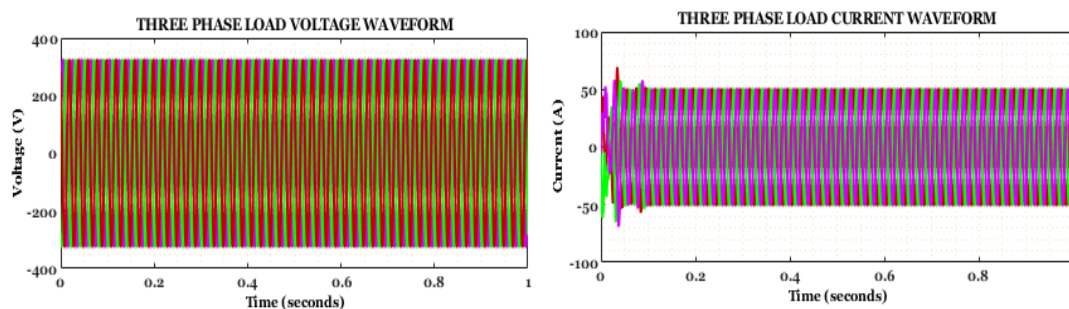


Figure 17. Three-phase load current waveform.

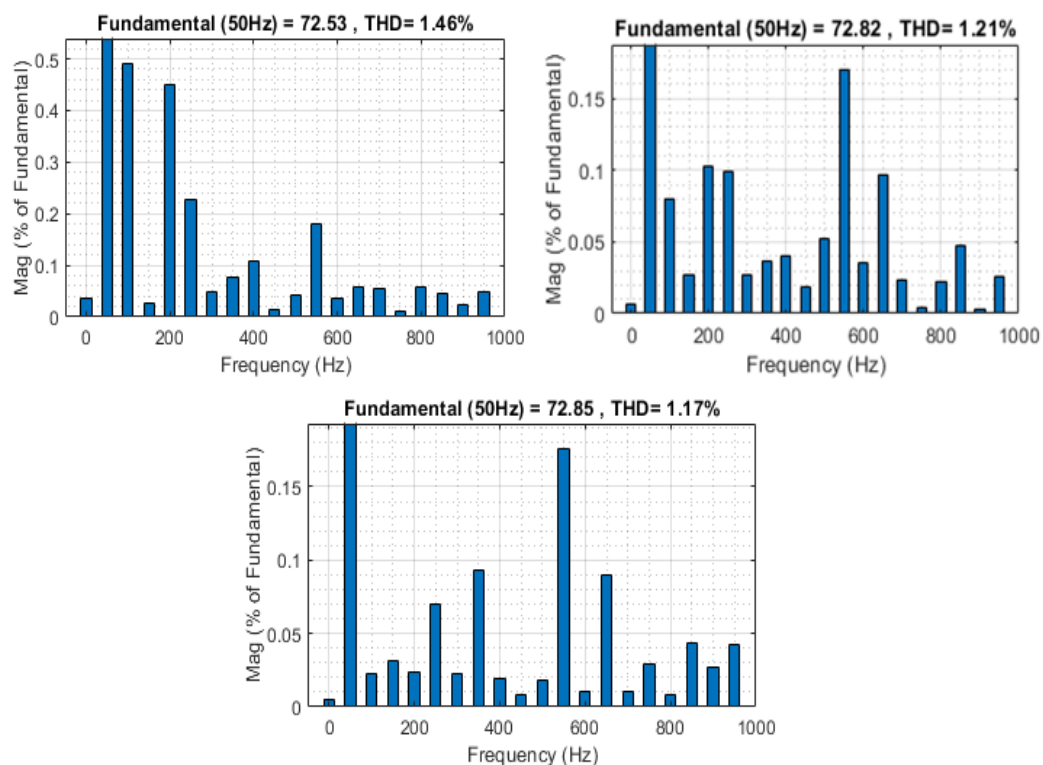


Figure 18. THD waveforms.

Figure. 17 exhibits the three-phase load current and voltage waveforms. Waveform of voltage is a balanced, sinusoidal waveform across all three phases with uniform amplitude and phase relationship, reflecting effective voltage regulation with minimal harmonic distortion. The current waveform at the present time is sinusoidal with evenly spaced phase and zero ripple, affirming to the efficiency of the converter in providing high-quality current to the load. The smooth and coordinated shape of both voltage and current waveforms indicates converter's highly optimized control strategy and stiff design, which provides guaranteed and ripple-free charging performance for up-to-date EV applications.

Figure. 18 reveals the harmonic spectrum analysis of the output current of the designed low-THD rippleless PFC converter, consists of three phase such as R-phase, Y-phase and B-phase of THD waveforms, each showing the magnitude of harmonics as a percentage of fundamental frequency (50 Hz), to 1000 Hz. The B-phase has a THD of 1.17%, the Y-phase 1.21%, and the R-phase 1.46%, all three having a fundamental component at approximately 72.5 units, ensuring the efficient suppression of higher-order harmonics by the converter, which means there is little distortion in the current output. The step-by-step decrease in THD through the graphs emphasizes the influence of fine-tuned control mechanisms and filtering methods utilized in the converter design. Low THD values are vital for grid compliance, improving power quality, and achieving efficient and secure EV battery charging.

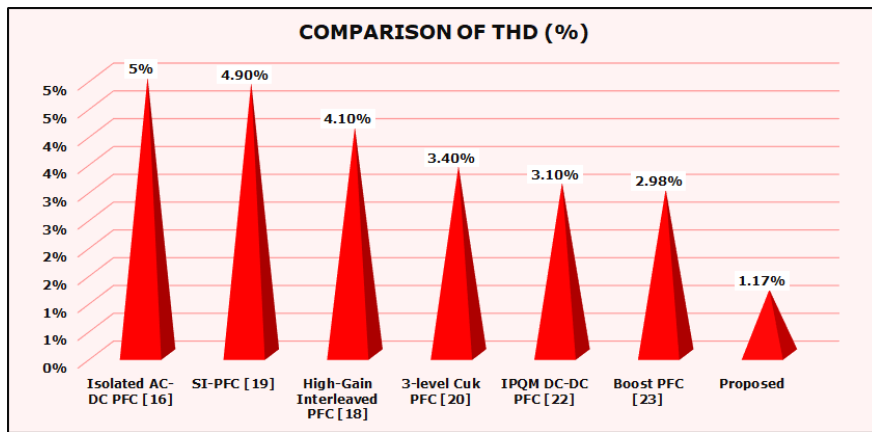


Figure 19. Comparison of THD.

Figure. 19 presents the comparison of THD for five PFC converter topologies demonstrating the better performance of the developed rippleless PFC converter for high-performance EV charging. The proposed rippleless PFC converter far surpasses all others with an impressively low THD of only 1.17%. The findings confirm the proposed PFC converter's ability to supply clean, efficient, and ripple-free power, which is extremely appropriate for next-generation EV charging infrastructure where power quality and battery protection are critical.

Table 2. Comparative analysis of PF.

PFC Converter	Power Factor
Totem-pole Bridgeless PFC [17]	0.99%
SI-PFC [19]	0.99
3-level Cuk PFC [20]	0.99
SRM-PFC [21]	0.99
Boost PFC [23]	0.99
Proposed	1.00

Table. 2 represents the comparative analysis of power factor performance among conventional with proposed Rippleless PFC converter, it has a unity power factor of 1.00, indicating optimal synchronization of input voltage and current waveforms. This unity power factor demonstrates the superior control strategy and ability of ripple elimination of the converter, rendering it extremely appropriate for high-efficiency EV charging where power quality is paramount.

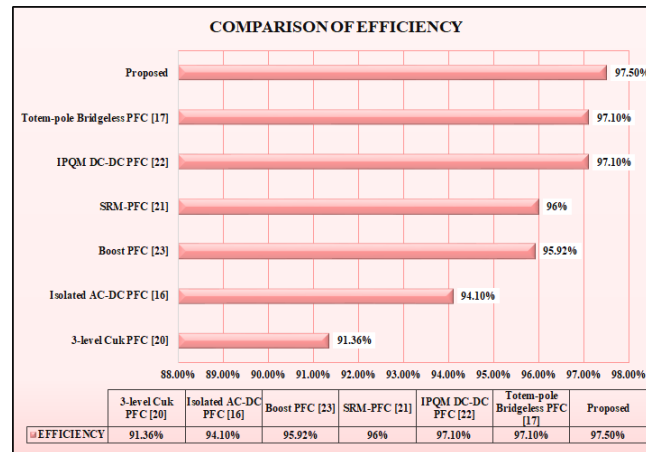


Figure 20. Comparison of converter efficiency.

Figure. 20 exhibits efficiency comparison of different PFC converter for attaining better performance, out of conventional converter methods, proposed rippleless PFC converter has the highest efficiency of 97.50%, highlighting its efficient design and low switching losses. The proposed rippleless topology and sophisticated control method are responsible for both high efficiency and enhanced power quality.

5. CONCLUSION

A high-performance battery charger with improved power quality has been designed and its performance verified by simulation using an emulated resistive load. The system exhibits better source current features and optimized charging characteristics, leading to increased battery lifetime. The output DC link voltage is well-controlled within limits, and charging process is regulated using a hysteresis control strategy realized using PI control. The dynamic response of the charger has been analyzed under different AC mains voltage levels and low load conditions through MATLAB/Simulink-based simulations. Harmonic content of input current is in accordance with IEEE regulations, keeping THD (1.17%) within limits. The proposed PFC-based charger achieves smooth and high efficiency of 97.5% battery charging while optimizing real power transfer by reshaping the input current waveform. Besides that, the flexibility of the proposed converter for EV charging systems three-phase and bidirectional has been thought through. For higher power level systems, the control strategy is upgraded by using coordinated multi-phase hysteresis, PI loops, whereas galvanic isolation is strengthened with modular high-frequency transformers. These changes maintain low THD and unity power factor, thus enabling the scalable and dependable operation of advanced EV charging infrastructures.

Author Contributions:

Conceptualization: Adapa Sudheer Kumar

Data Curation: Adapa Sudheer Kumar

Methodology: V. Suresh, Daggu Veera Venkata Chaitanya, Depati Veera Venkata Sai, Gavara Sai Babu & Adapa Sudheer Kumar

Project administration: V. Suresh, Daggu Veera Venkata Chaitanya, Depati Veera Venkata Sai & Gavara Sai Babu

Supervision: V. Suresh, Daggu Veera Venkata Chaitanya, Depati Veera Venkata Sai & Gavara Sai Babu

Validation: V. Suresh, Daggu Veera Venkata Chaitanya, Depati Veera Venkata Sai & Gavara Sai Babu

Writing-original draft: Adapa Sudheer Kumar

Writing-review & editing: V. Suresh, Daggu Veera Venkata Chaitanya, Depati Veera Venkata Sai, Gavara Sai Babu & Adapa Sudheer Kumar

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